

About the College

Dr. Mahalingam College of Engineering and Technology (MCET) was established in the year 1998 by Dr.M.Manickam with a view to commemorate the 75th birth day of his beloved father Arutchelvar Dr. N. MAHALINGAM with a mission to impart high quality competency based education in Engineering & Technology to the younger generation to acquire the required skills and abilities to face the challenging needs of the industry around the globe. MCET is a self-financing, co- educational Autonomous Engineering College and it is approved by All India Council for Technical Education (AICTE), New Delhi & affiliated to Anna University, Chennai. The Institution has been accredited by NAAC with A++ and 7 UG programmes(CSE,EEE,EIE,ECE,CIVIL,Mechanical, Automobile) are accredited with Tier I by National Board of Accreditation (NBA). MCET currently offers 10 UG 6 PG and 5 doctoral programs in Engineering, Technology and Science.

About the Department

The Department of Electronics and Communication Engineering was established in the year 1998 and offers B.E (ECE) and M.E (Communication Systems) approved by AICTE, affiliated to Anna University, and accredited by NBA. The department has experienced and qualified faculty members who are fully committed to teaching, research and dedicated to impart quality education to the students. The students have access to well equipped, state-of-the-art laboratories. The department is focusing on research activities in the predominant areas on Communication and Networking, RF, VLSI, image and signal processing. The department is conducting many programmes to bring research experts from various industries and institutions, to share their knowledge in their area of expertise.

Chief Patron:

Dr. M. Manickam,
Chairman, MCET

Patron:

Shri. M. Hari Hara Sudhan,
Correspondent, MCET

Chairman:

Dr. C. Ramaswamy,
Secretary, NIA Educational Institutions

Co- Chairman:

Dr. A. Rathinavelu
Principal, MCET

Conveners:

Dr. R. Sudhakar
Professor and Head - ECE
Dr. K.N. Vijeyakumar
Associate Professor – ECE

Organizing Secretaries:

Ms. R. Sherine Jenny, AP(SS)
Ms. S. Kalaiselvi, AP

Committee Members:

Dr. C. Kalamani, AP (SS)
Ms. V. Bhuvaneshwari, AP
Ms. D. Reka, AP
Ms. N. Sugirtham, AP
Ms. S. Sugunavathy, AP
Mr. E. Vinoth, AP
Ms. T. Sathiyapriya, AP
Ms. M. Abirami, AP



AICTE Sponsored Two Weeks FDP on "Network Security and CMOS Mixed Signal Architectures " 27th May 2019 – 9th June 2019



Organized by
Department of Electronics and
Communication Engineering



**Dr. MAHALINGAM COLLEGE OF ENGINEERING
AND TECHNOLOGY**

(An Autonomous Institution)

(Accredited by NBA, NAAC with 'A++' Grade)

Pollachi-642003 Coimbatore (Dt), Tamilnadu

Phone: +91-4259-236030/40/50 Fax: +91-4259-236070

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About the Programme

Network security has been important research topic at present due to wide use of secure data transmission in real time viz., banking, insurance, online transactions, markets, telecommunication, electrical power distribution, health and medical fields, nuclear power plants, space research and satellites. The recent initiatives viz., digital India, demonetisation and encouragement of online transactions by Indian Government further aids the importance and necessity of security in data transmission. In addition, the demand for portability necessitates the design of low power hardware for data security as they are mostly battery operated. This Faculty Development Programme is organized to provide an awareness about the need for network security and design of low cost hardware for its implementation.

Topics to be Covered:

- IC Design Flow, Process Integration, IC Fabrication
- Layout Techniques, Standard Cell design
- Design of algorithms for Image and Data Encryption
- Security Protocols and mechanisms, Cryptography algorithms, issues of Symmetric cipher cryptanalysis
- Internet of Things-Privacy and Security Research aspects and direction

Hands-on Sessions:

- Modeling, Simulation of data encryption/ decryption systems.
- Analog IC design flow
- Digital IC design flow
- Layout optimization based on performance metrics

Experts:

Resource persons from Semiconductor Laboratory (Department of space)-Chandigarh, Mentor Graphics - Siemens Business, Core EL Technologies, EmbDes Technologies-Bangalore and academicians from reputed institutions.

Eligibility:

Faculty members and Research Scholars from AICTE recognized institutions can attend.

Registration & Participation:

Registration fee is Rs.1000/- for faculty members and Research Scholars. The mode of payment is through Demand Draft drawn in favour of "The Principal, Dr. Mahalingam College of Engineering and Technology" payable at Pollachi. Duly filled registration form along with DD must reach us on or before 23.05.2019. This amount will be refunded to the participants who attend the program completely. The number of participants is limited to 40 and the selection is on first-come-first-serve basis.

Accommodation Details:

Accommodation will be provided on limited basis with prior request for outstation participants. The reimbursement of travel expenses will be made as per AICTE guidelines. TA will be provided to the outstation participants on submission of the necessary documents.

Address for Communication

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Department of Electronics and

Communication Engineering,

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Pollachi - 642003

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REGISTRATION FORM

AICTE Sponsored Two Weeks FDP on
"Network Security and CMOS Mixed Signal
Architectures "

27th May 2019 - 9th June 2019

(To be filled in Block Letters)

Name :

Designation :

Department :

Institution :

Address for Communication :

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Pincode :

Phone/Mobile:

Email id :

I have enclosed DD in favour of
"The Principal, Dr. Mahalingam College of
Engineering and Technology" payable at Pollachi for
an amount of Rs.1000/- towards registration fee.

Demand Draft Details:

DD No & Date :

Bank Name :

Branch Name :

Signature of the
Candidate

Signature of the
Head of the Institution
with seal